Freescale Semiconductor
Technical Data

Document Number: MRF5S21045N
Rev. 4.1, 12/2009

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF5S21045NR1
MRF5S21045NBR1

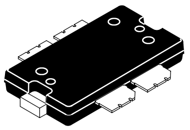
2110-2170 MHz, 10 W AVG., 28 V
2 x W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

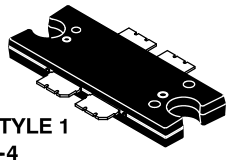
- Typical 2-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 500 mA, P_{out} = 10 Watts Avg., f = 2112.5 MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 14.5 dB
  - Drain Efficiency — 25.5%
  - IM3 @ 10 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
  - ACPR @ 5 MHz Offset — -39 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 45 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF5S21045NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF5S21045NBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	130 0.74	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 45 W CW Case Temperature 79°C, 10 W CW	$R_{\theta JC}$	 1.35 1.48	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

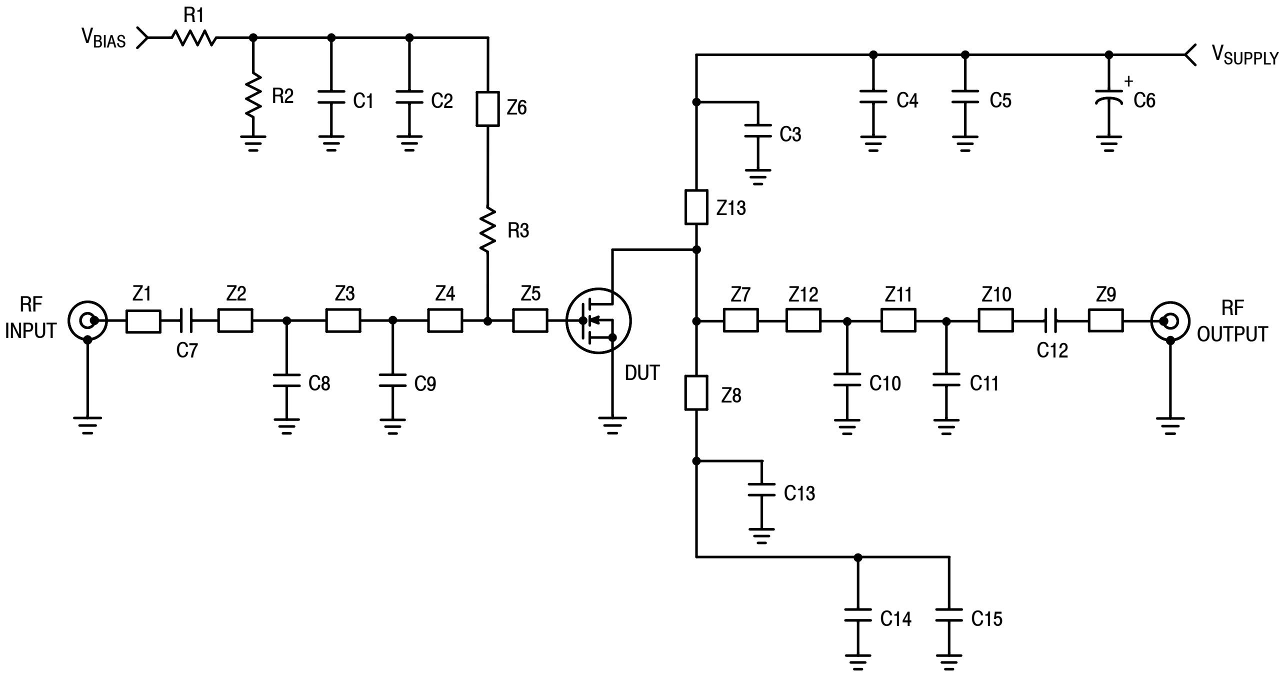
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	2	—	3.5	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2	3.8	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.2 Adc)	$V_{DS(on)}$	0.2	—	0.35	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.2 Adc)	g_{fs}	—	3.2	—	S
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.9	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg., f1 = 2112.5 MHz, f2 = 2122.5 MHz, 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 measured in 3.84 MHz Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	13.5	14.5	16.5	dB
Drain Efficiency	η_D	24	25.5	—	%
Intermodulation Distortion	IM3	—	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	—	-39	-37	dBc
Input Return Loss	IRL	—	-12	-9	dB

1. Part is internally matched both on input and output.



Z1, Z9	0.250″ x 0.080″ Microstrip	Z7	0.500″ x 1.000″ Microstrip
Z2	0.987″ x 0.080″ Microstrip	Z8, Z13	0.270″ x 0.080″ Microstrip
Z3	0.157″ x 0.080″ Microstrip	Z10	0.789″ x 0.080″ Microstrip
Z4	0.375″ x 0.080″ Microstrip	Z11	0.527″ x 0.080″ Microstrip
Z5	0.480″ x 1.000″ Microstrip	Z12	0.179″ x 0.080″ Microstrip
Z6	0.510″ x 0.080″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, $\varepsilon_r = 2.55$

Figure 1. MRF5S21045NR1(NBR1) Test Circuit Schematic

Table 6. MRF5S21045NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	220 nF Chip Capacitor (1812)	1812Y224KAT	AVX
C2, C3, C7, C12, C13	6.8 pF 100B Chip Capacitors	ATC100B6R8CT500XT	ATC
C4, C5, C14, C15	6.8 μF Chip Capacitors (1812)	C4532X5R1H685MT	TDK
C6	220 μF, 63 V Electrolytic Capacitor, Radial	2222-136-68221	Vishay
C8, C10	1 pF 100B Chip Capacitors	ATC100B1R0BT500XT	ATC
C9	1.5 pF 100B Chip Capacitor	ATC100B1R5BT500XT	ATC
C11	0.5 pF 100B Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

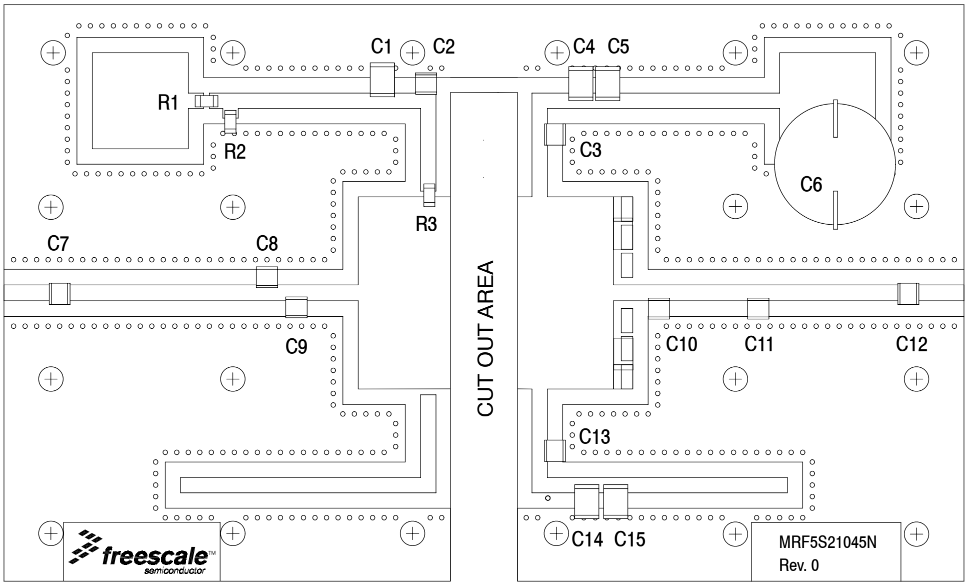


Figure 2. MRF5S21045NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

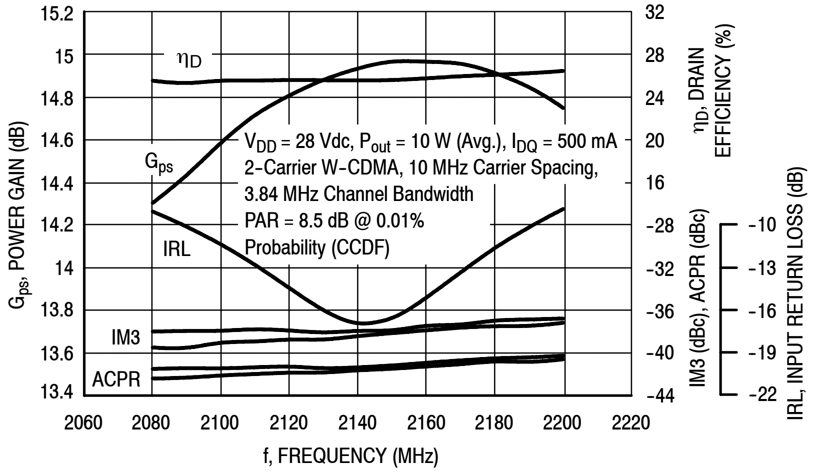


Figure 3. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 10 Watts

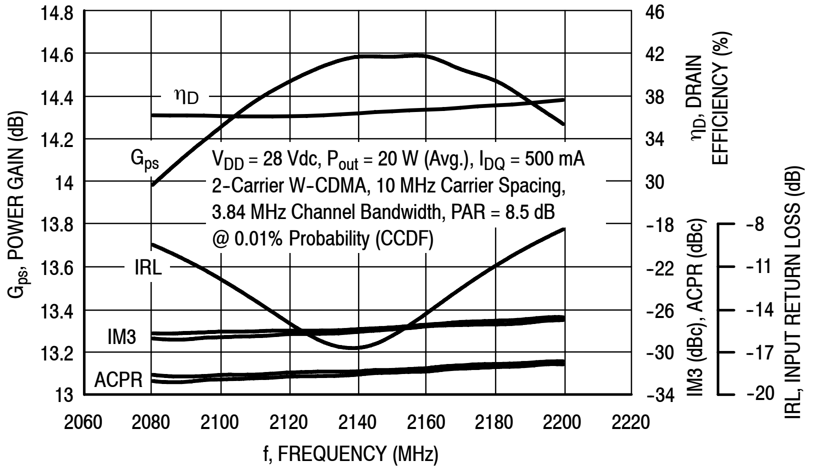


Figure 4. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 20 Watts

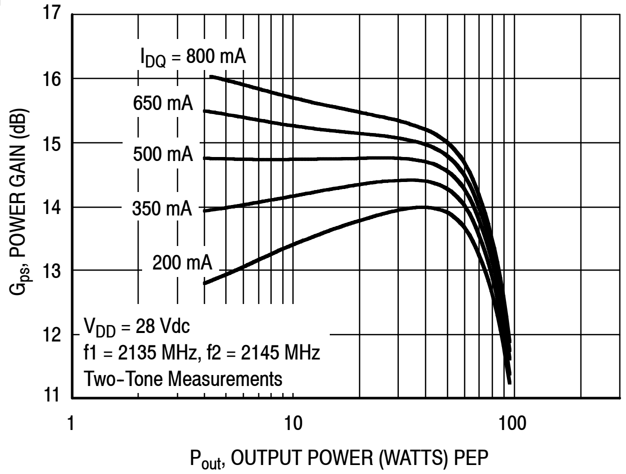


Figure 5. Two-Tone Power Gain versus Output Power

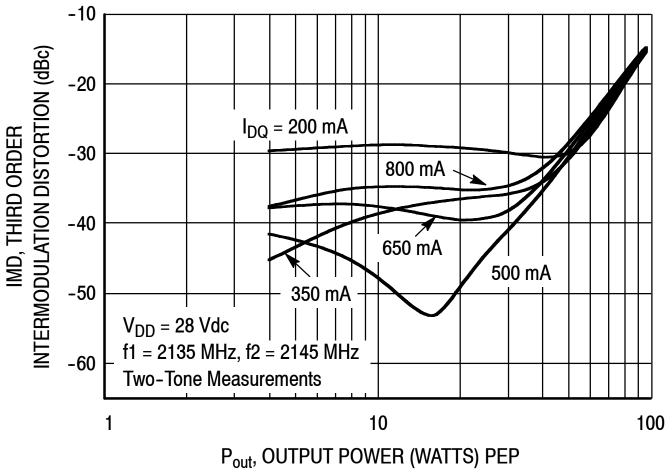


Figure 6. Third Order Intermodulation Distortion versus Output Power

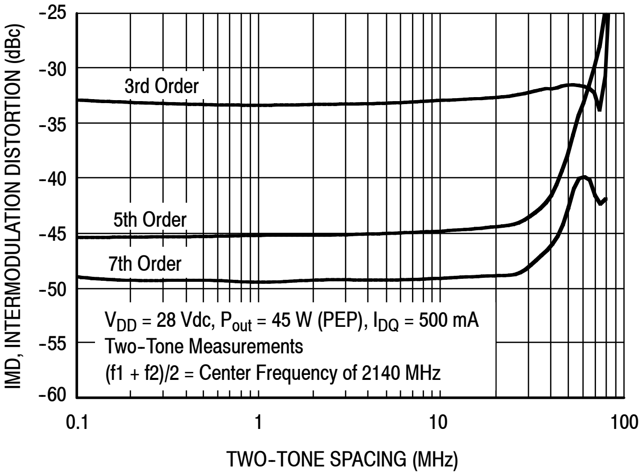


Figure 7. Intermodulation Distortion Products versus Tone Spacing

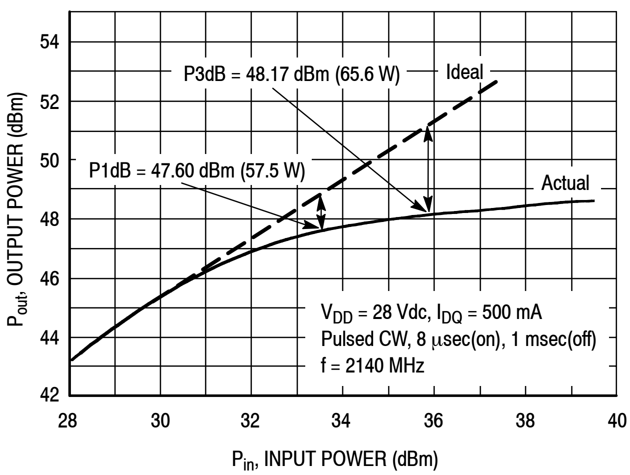


Figure 8. Pulse CW Output Power versus Input Power

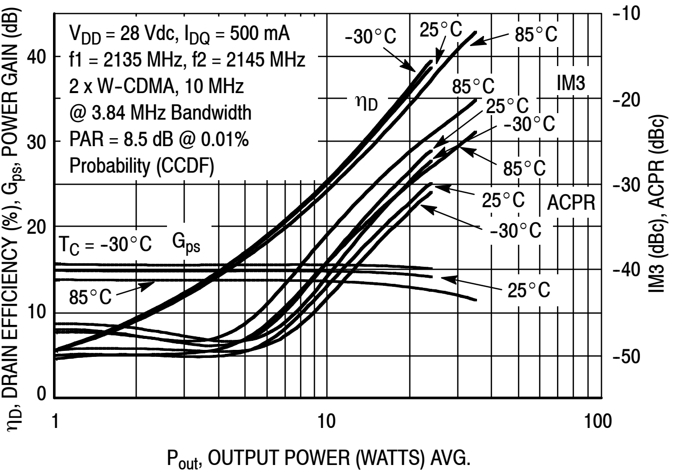


Figure 9. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

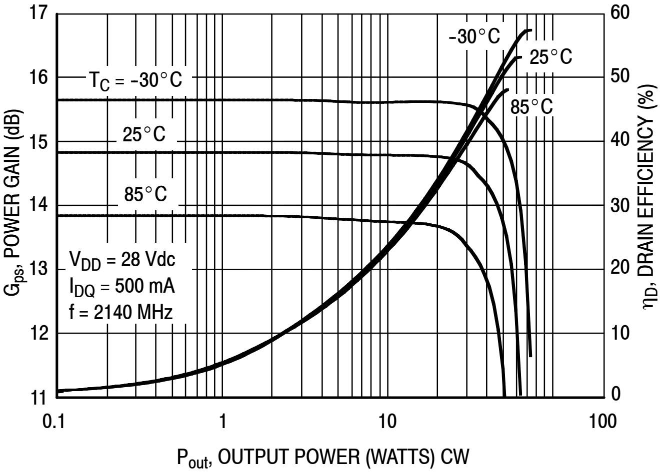


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

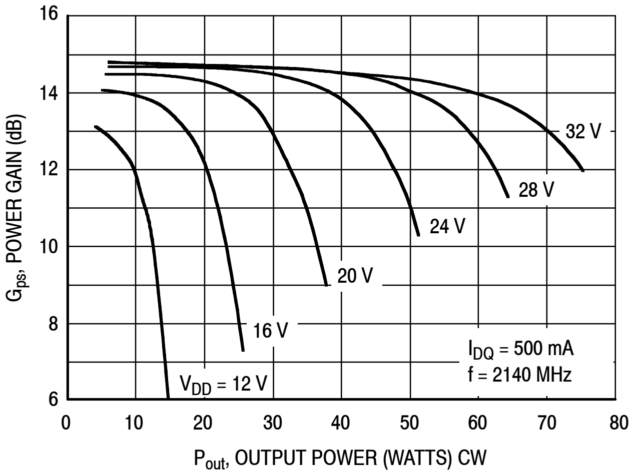
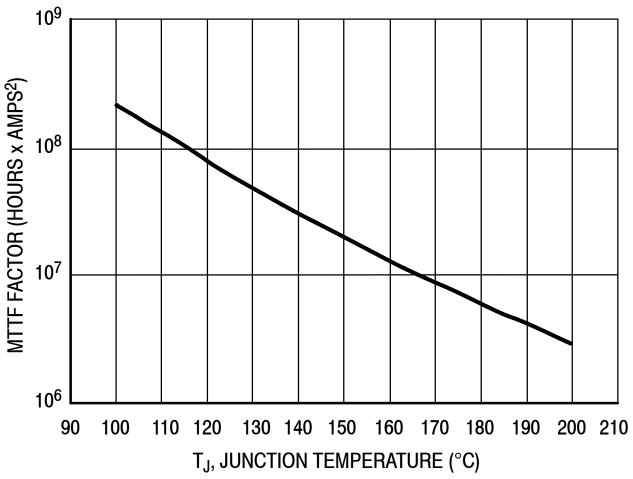


Figure 11. Power Gain versus Output Power

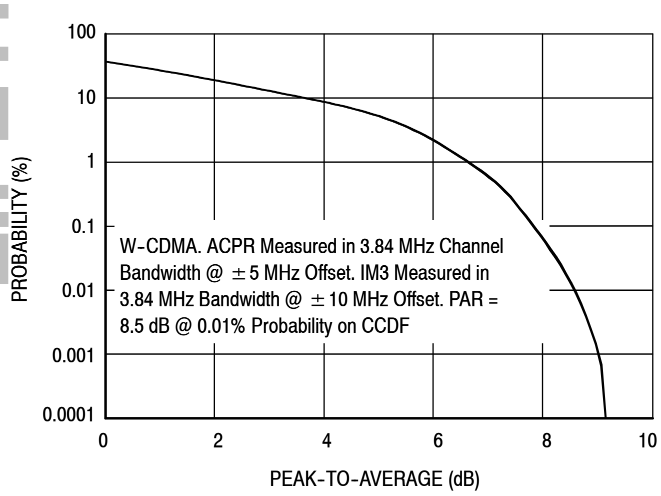
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 12. MTTF Factor versus Junction Temperature

W-CDMA TEST SIGNAL



W-CDMA. ACPR Measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 Measured in 3.84 MHz Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF

Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal

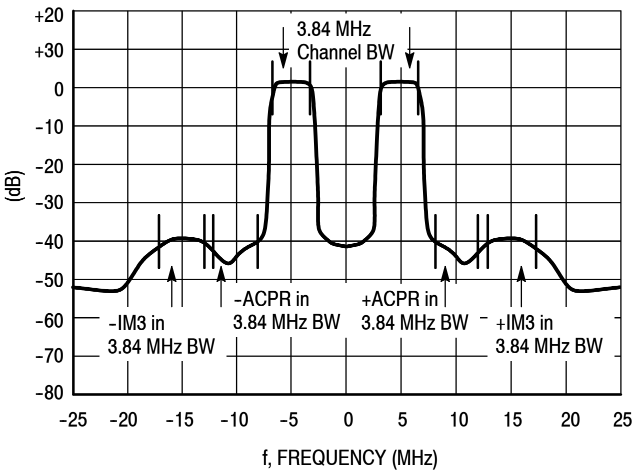
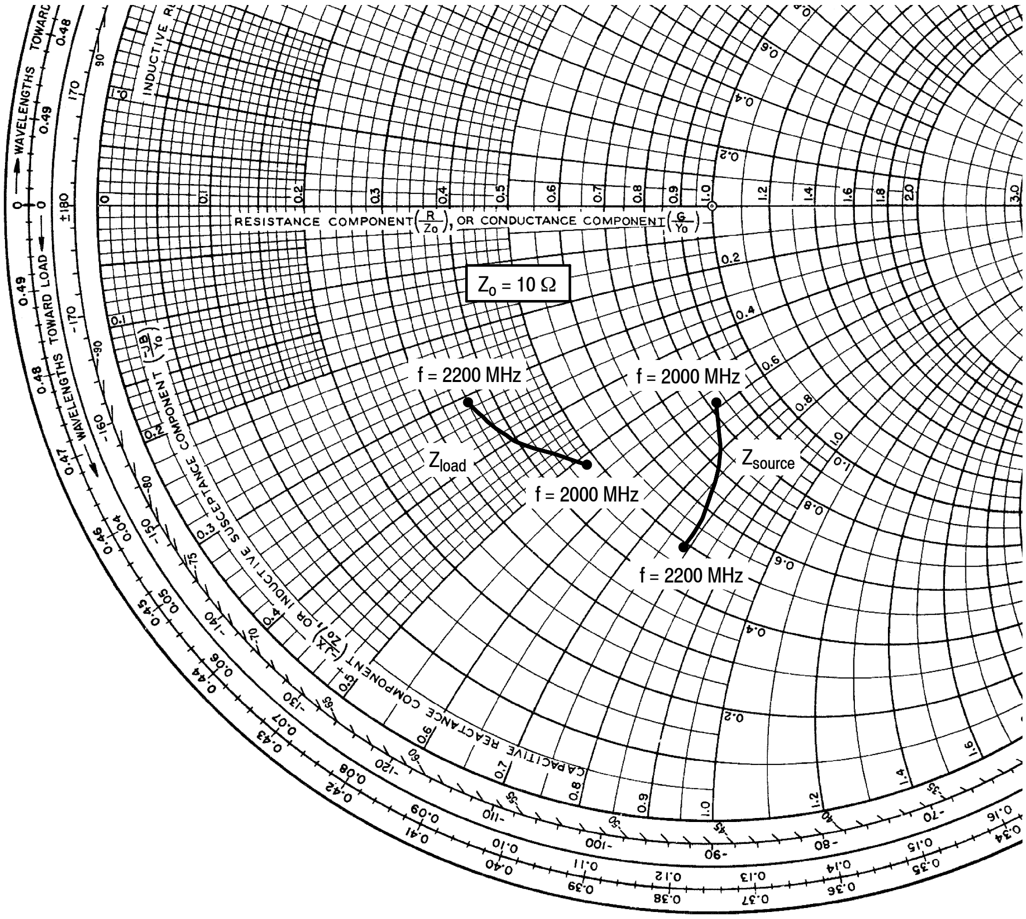


Figure 14. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2000	8.15 – j5.91	4.78 – j5.19
2110	7.07 – j7.32	4.04 – j4.14
2140	6.28 – j7.71	3.81 – j3.69
2170	5.61 – j7.85	3.69 – j3.39
2200	4.92 – j7.85	3.57 – j3.11

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

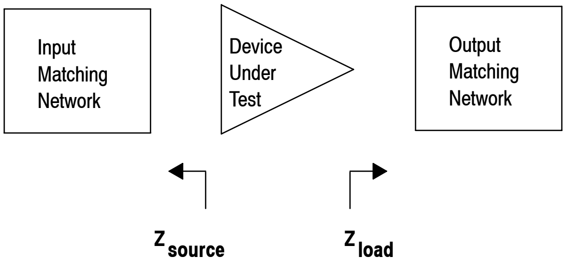
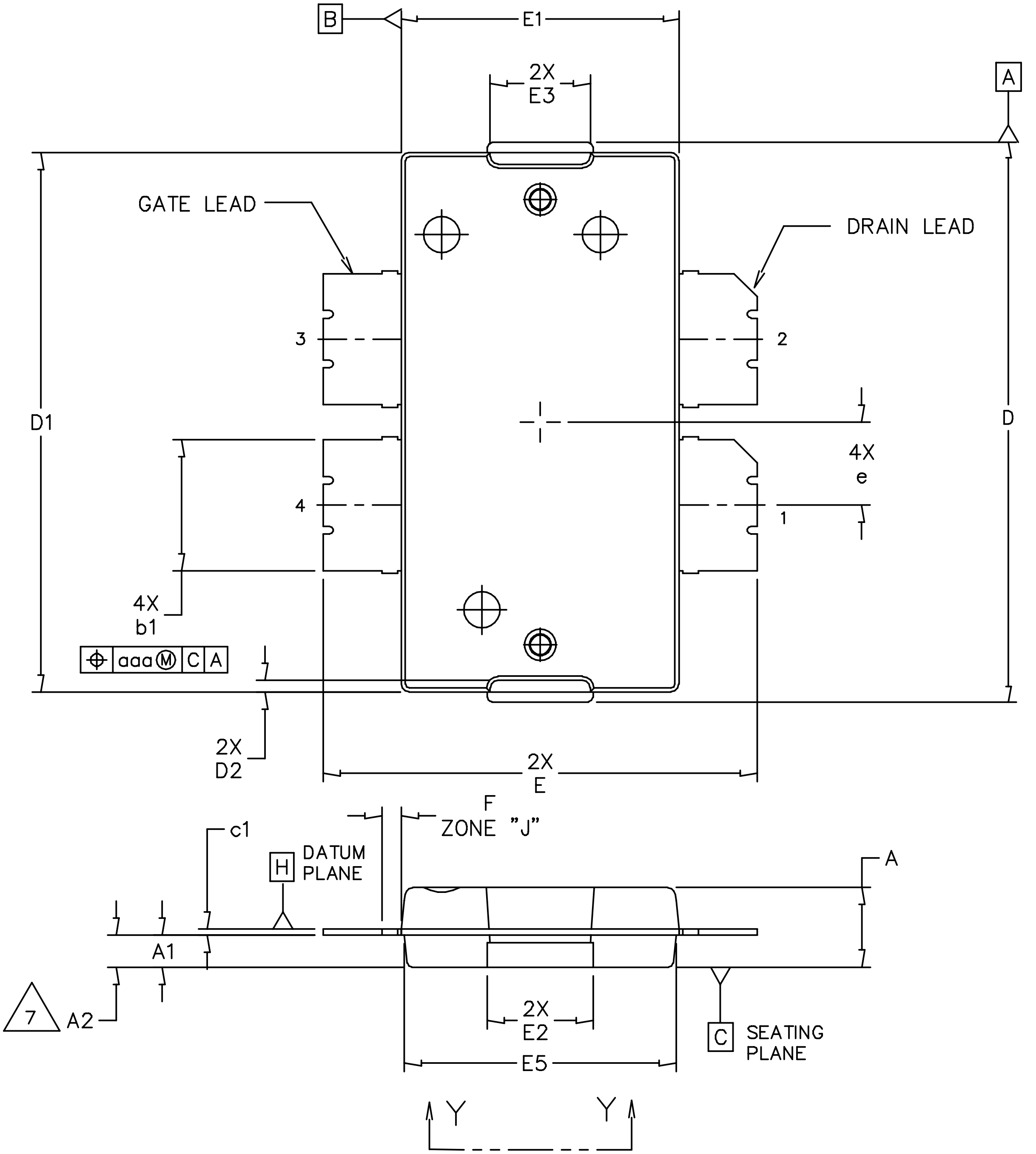


Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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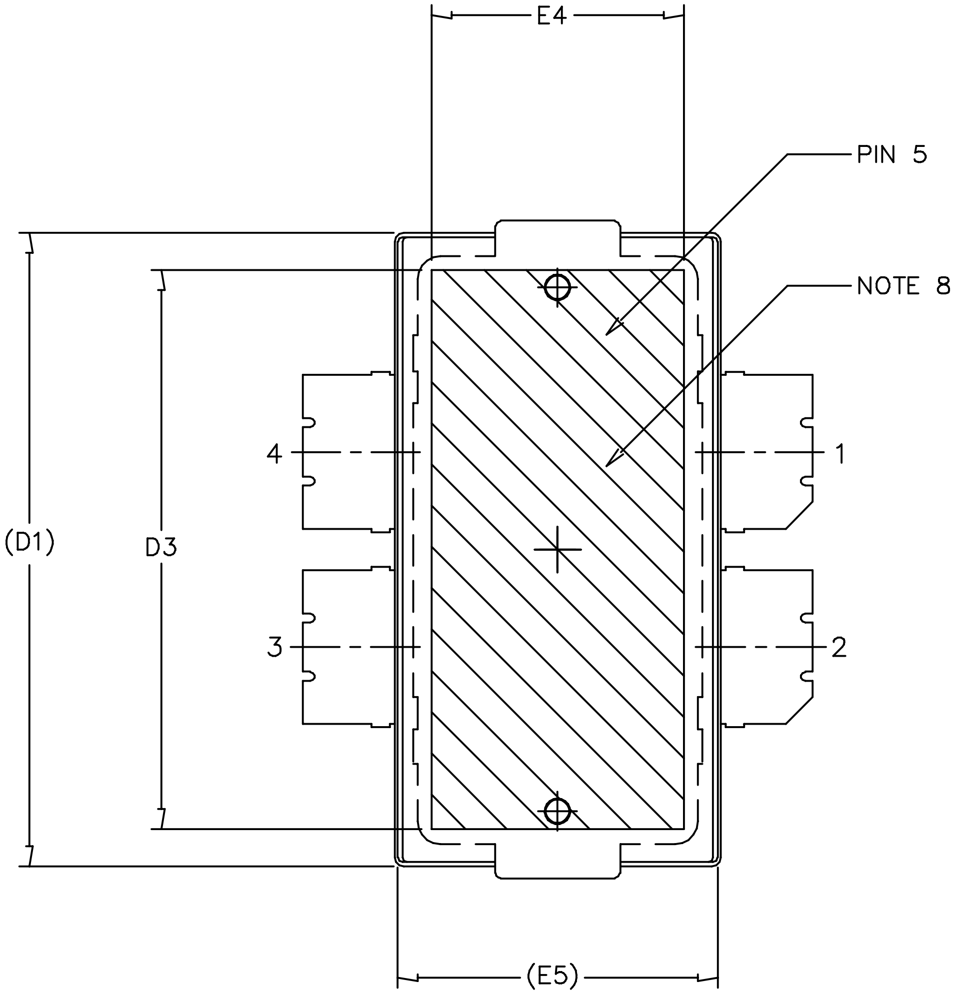
	STANDARD: NON−JEDEC		



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	CASE NUMBER: 1486–03	13 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 - DRAIN   PIN 2 - DRAIN
PIN 3 - GATE   PIN 4 - GATE
PIN 5 - SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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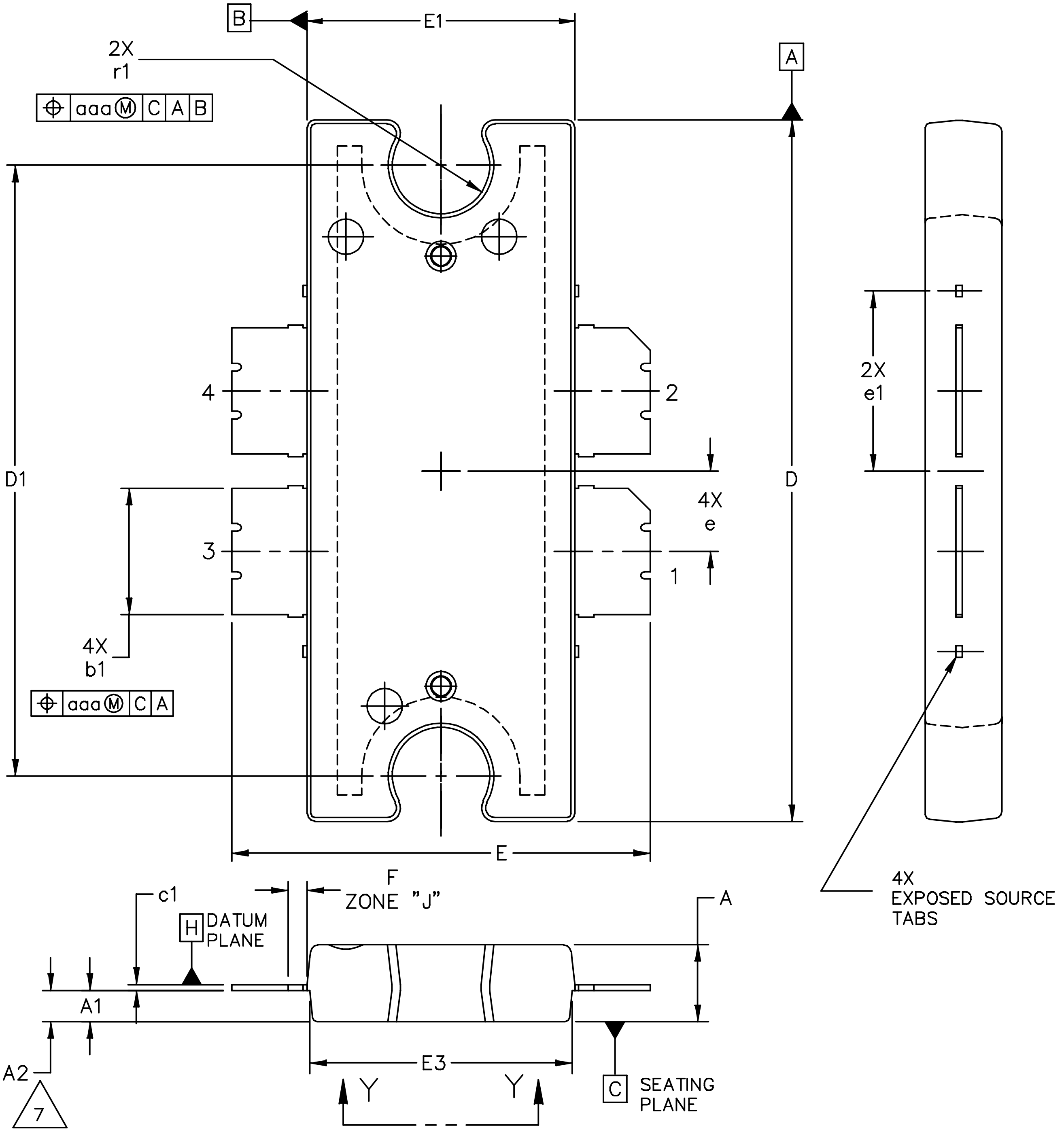

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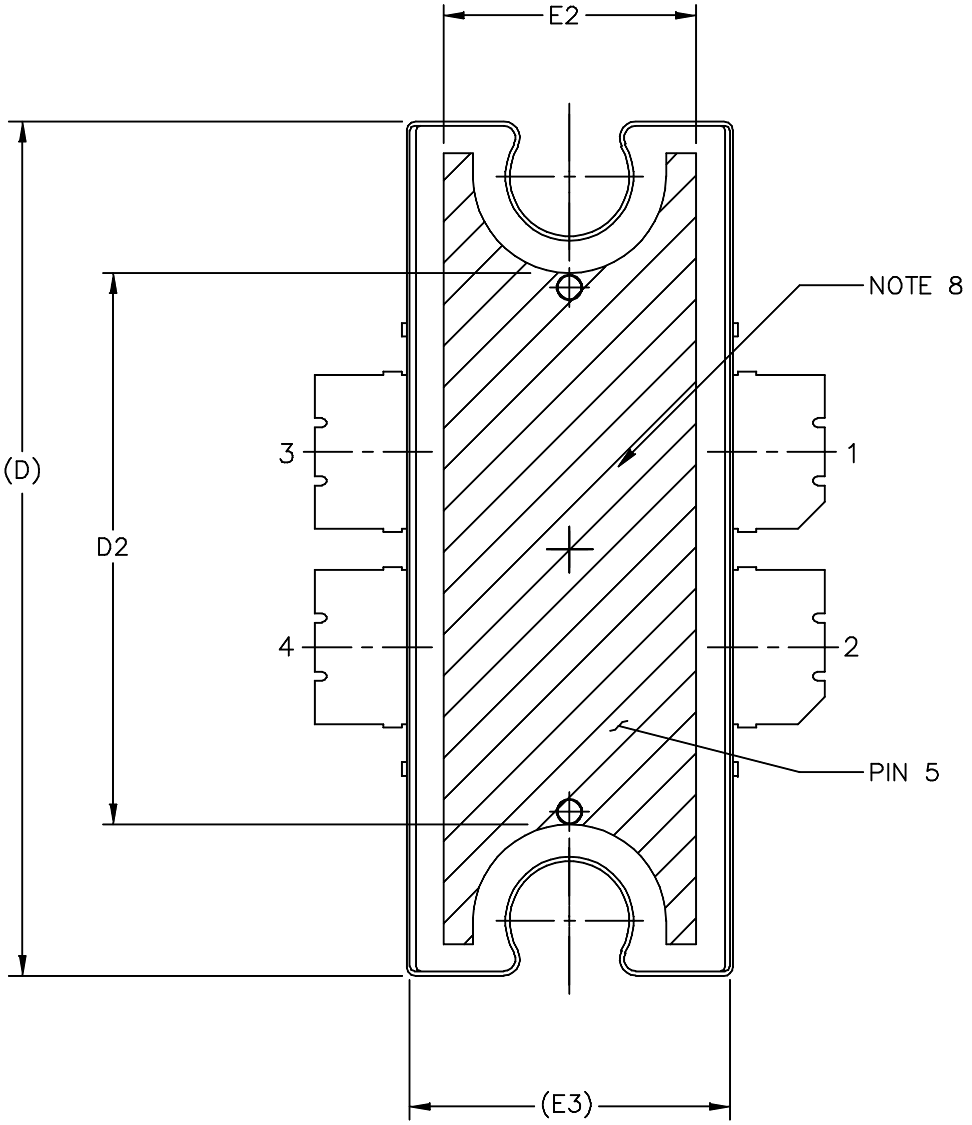

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	CASE NUMBER: 1484-04	31 AUG 2007
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 − DRAIN PIN 2 − DRAIN
PIN 3 − GATE PIN 4 − GATE
PIN 5 − SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	−−−	15.24	−−−	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	−−−	6.86	−−−					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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CASE NUMBER: 1484−04

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STANDARD: NON−JEDEC

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
4	Oct. 2008	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2 • Updated Part Numbers in Table 6, Component Designations and Values, to latest RoHS compliant part numbers, p. 3 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 9-11. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 12-14. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations. • Added Product Documentation and Revision History, p. 15
4.1	Dec. 2009	• Corrected data sheet to reflect RF Test Reduction frequency described in Product and Process Change Notification number, PCN12779, p. 2

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