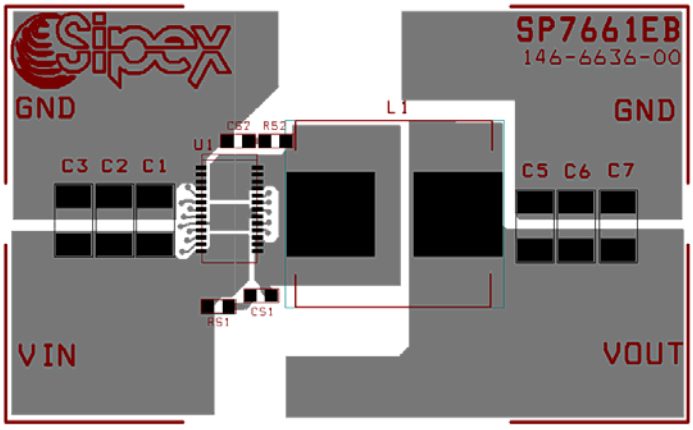
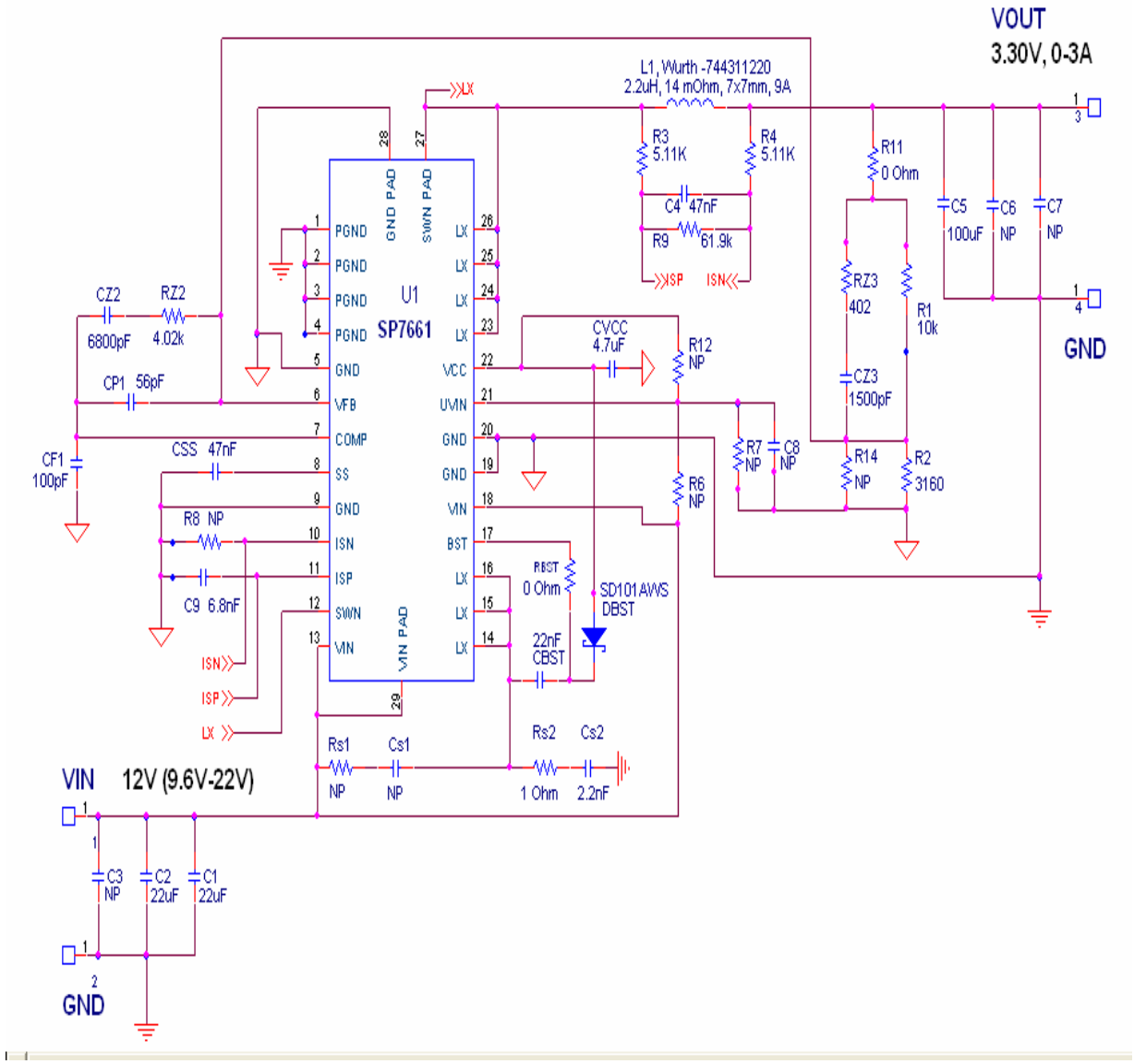
- Easy Evaluation of the SP7661ER 0 to 3A Output Synchronous Buck Converter
- Built in Power MOSFETs
- UVLO Detects Both VCC and VIN
- Highly Integrated Design, Minimal Components
- High Efficiency: up to 90%
- Feature Rich: UVIN, Programmable Soft Start, Built In VCC Supply Output Short Circuit Protection and Current Limiting



SP7661EB Schematic



Using the Evaluation Board

1) Powering Up the SP7661EB Circuit

Connect the SP7661 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the "VIN" and "GND" posts. Connect a Load between the VOUT and GND posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

VOUT ripple can best be seen by touching the probe tip to the pad for C5 and the scope GND collar touching Output GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7661 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7661 can be set to other output voltages. The relationship in the Equation 1 is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Note, due to the common mode voltage range of the current sense amplifier, output voltages greater than 3.3V are only possible if the current sense is disabled. To disable current limit, remove R3 and R4. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$R2 = \frac{R1}{\left(\frac{Vout}{.80V} - 1\right)} \qquad \text{Equation 1}$$

Where R1 = 10kΩ and for V_{OUT} = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 & R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $10k\Omega \leq R1 \leq 100k\Omega$ for overall system loop stability.

Note that since the SP7661 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7661ER provides short circuit protection by sensing V_{OUT} at GND. The current limit of the converter is set to about 5.5A which is accomplished by sensing the current through the inductor. To adjust the current limit, follow Equations 2 and 3 to set the current limit accordingly. The current limit should be set to about 50% higher than the maximum output current that is desired. This will prevent the part from accidentally triggering the current limit during large transient load steps.

Adjusting the current upwards is done by adjusting resistor R9.

$$R9 = \frac{60mV \cdot (R3 + R4)}{I_{MAX} \cdot (DCR - 60mV)} \qquad \text{Equation 2}$$

Where DCR is the Inductor winding resistance
I_{MAX} is the desired output current

Adjusting the current downwards is controlled by adjusting R8.

$$R8 = R4 \cdot \left(\frac{(Vout - 60mV) + (Imax \cdot DCR)}{60mV - (Imax \cdot DCR)} \right) \quad \text{Equation 3}$$

Where DCR is the Inductor winding resistance and
I_{MAX} is the desired output current

Further details on the current limit can be found in the SP7661 data sheet. For the Wurth Inductor on this demo board, DCR= 14mΩ nominal.

POWER SUPPLY DATA

The SP7661ER is designed with an accurate 2.0% reference over line, load and temperature. Figure 1 data shows a typical SP7661 evaluation board efficiency plot, with efficiencies up to 90% and output currents up to 3A. The output voltage ripple of less than 10mV at full load and the LX node are shown in figure 2. Figures 3 and 4 illustrate a 0A to 3A and 1A to 3A Load Step. Short circuit and current limit are shown in Figures 5 and 6. Typical startup characteristics into a full load and no load are shown in figure 7 and 8. All data was taken at $12V_{IN}$.

While data on individual power supply boards may vary, the capability of the SP7661ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

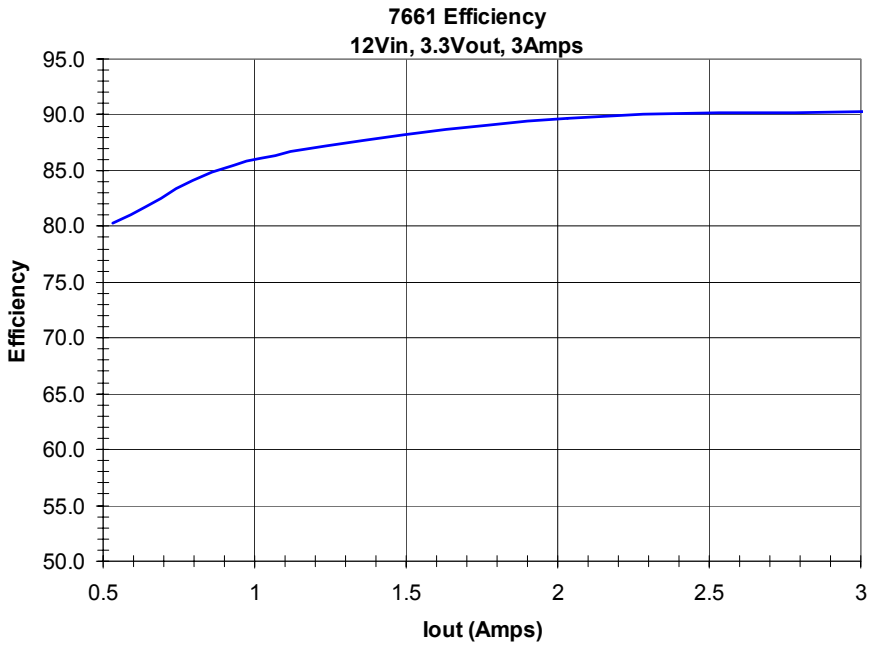


Figure 1. Efficiency vs. Load

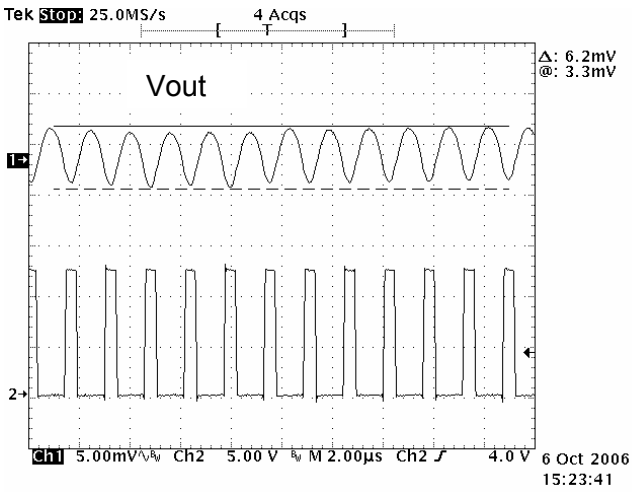


Figure 2. LX node output & ripple voltage

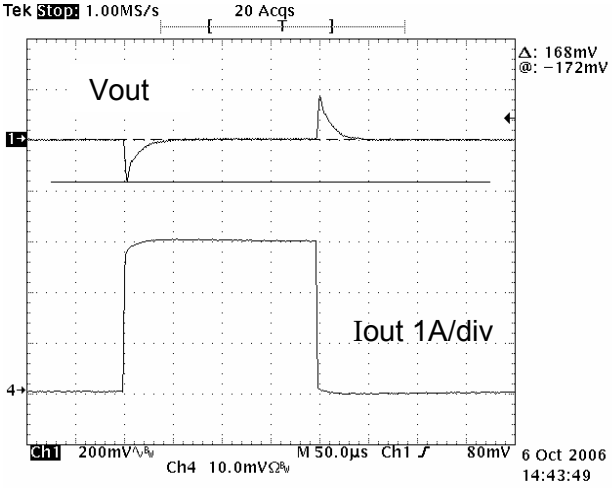


Figure 3. Load Step Response: 0->3A

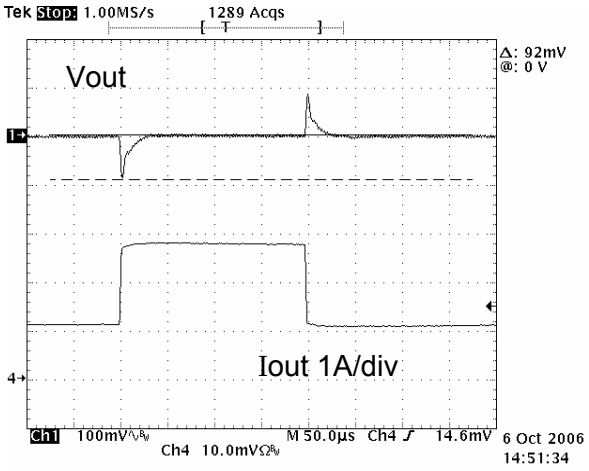


Figure 4. Load Step Response 1->3A

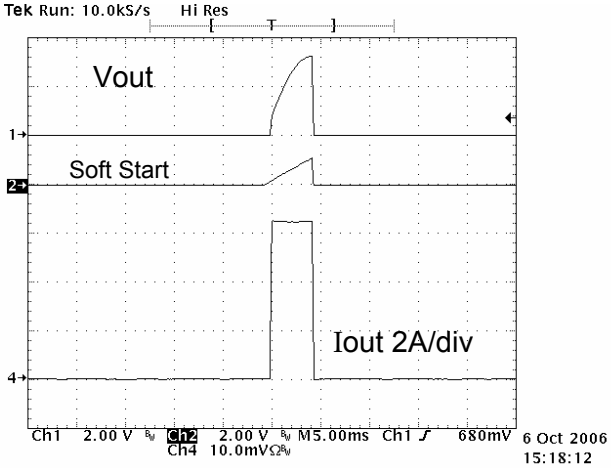


Figure 5. Current limit set point ~6A

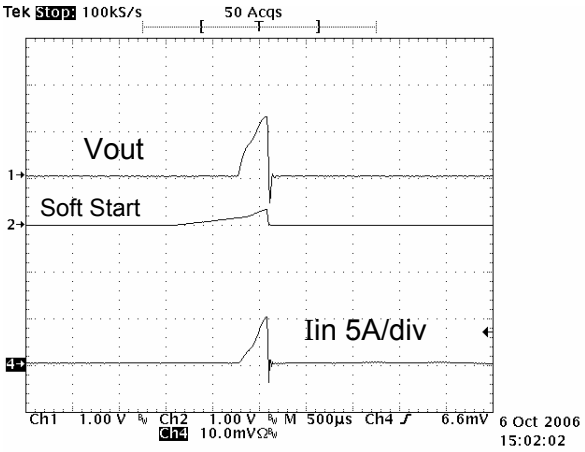


Figure 6. Output Short Circuit w/IIN

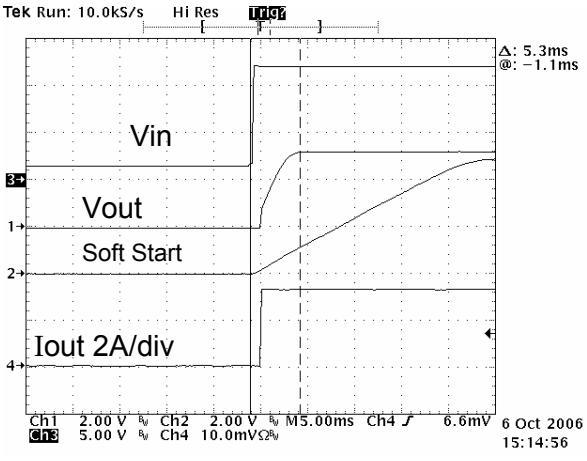


Figure 7. Startup into full load

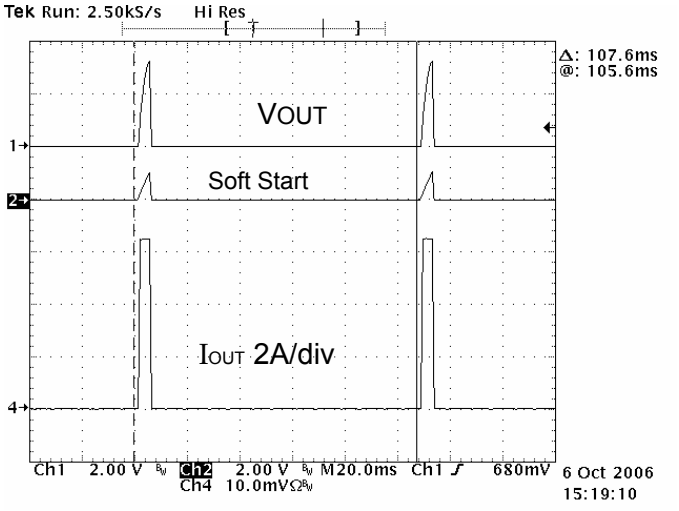


Figure 8. Current Limit Re-start Rate

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7661EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to cross over at the selecting frequency **fco**, the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7661EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** underdamped resonance double pole frequency.

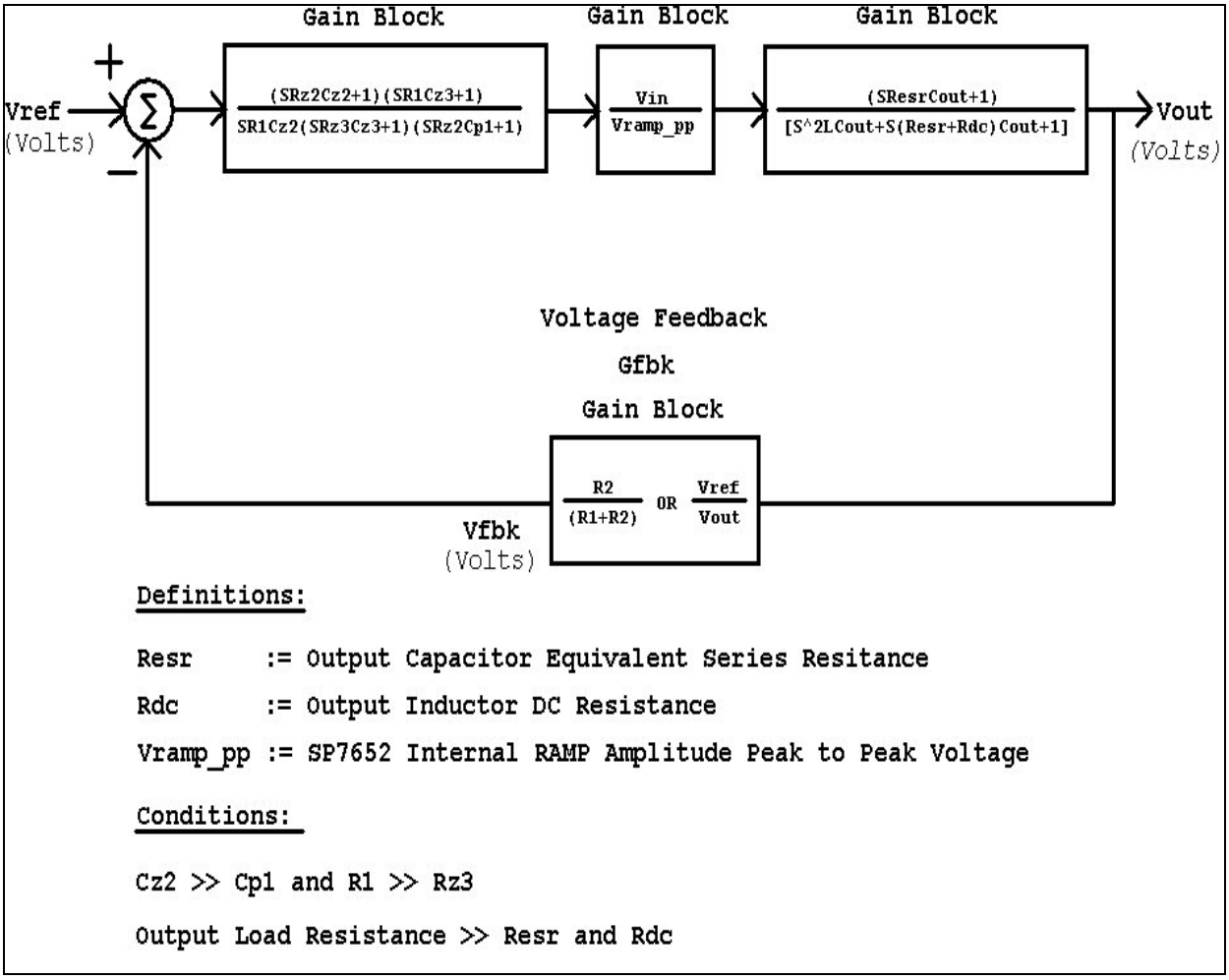


Figure 9. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows. As a particular example, consider for the following SP7661EB with a **Type III** Voltage Loop Compensation component selections:

Input requirements and inductor selection
Vin = 12V, we will use 12V as Vin max for this design.
Vout = 3.30V @ 0 to 3A load
Select **L = 2.2uH** => yield ≈ 60% of maximum 3A output current ripple.
Select **Cout = 100uF Ceramic** capacitor (Resr ≈ **3mΩ**) Given the performance of ceramic caps we will use ~80% of the output capacitance in calcualations.
fs = 600khz SP7661 internal Oscillator Frequency
Vramp_pp = 1.0V SP7661 internal Ramp Peak to Peak Amplitude

Step by step design procedures:

> Note: Loop Compensation component calculations discussed in this section are further elaborated in the application note #ANP16, "**Loop Compensation of Voltage-Mode Buck Converters".**
> These calculations shown here can be quickly iterated with the Type III Loop Compensation Calculator on the web at:
> www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

Choose $\mathrm{fco} = \mathrm{fs}/10$

$$\mathrm{fco} = 600\mathrm{Khz}/10 = 60\mathrm{Khz}$$

Calculate **fp_LC,** the double pole frequency of the filter

$$\mathrm{fp\_LC} = \frac{1}{2\pi(\sqrt{\mathrm{L}\cdot\mathrm{C}})}$$

$$\mathrm{fp\_LC} = \frac{1}{2\pi\cdot\sqrt{2.2\mathrm{uH}\cdot 80\mathrm{uF}}} = 11.99\mathrm{kHz} \approx 12\mathrm{kHz}$$

Calculate **fz_ESR** , the ESR zero frequency

$$\mathrm{fz\_ESR} = \frac{1}{2\pi\cdot\mathrm{Cesr}\cdot\mathrm{Cout}}$$

$$fz\_ESR = \frac{1}{2\pi\cdot(3m\Omega)\cdot(80\mu F)} = 663kHz$$

Select **R1** component value such that $10\mathrm{k}\Omega \le \mathrm{R1} \le 100\mathrm{k}\Omega$

R1 = 10kΩ, 1%

Calculate **R2** base on the desired VOUT

$$R2 = \frac{R1}{\left[\frac{Vout}{.8V}\right]-1}$$

$$R2 = \frac{10K\Omega}{\left[\frac{3.3V}{.8V}\right]-1} = 3200\Omega \approx 3160\Omega$$

Select the ratio of **RZ2 / R1** gain for the desired gain bandwidth (from above, we will use 60kHz)

$$RZ2 = R1 \cdot \left[\frac{Vramp\_pp}{Vin\_\max}\right] \cdot \left(\frac{fco}{fp\_LC}\right)$$

$$RZ2 = R1 \cdot \left[\frac{1V}{12V}\right] \cdot \left(\frac{60kHz}{12kHz}\right) = 4166\Omega \cong 4020\Omega$$

Calculate **CZ2** by placing the zero at ½ of the output filter pole frequency

$$CZ2 = \frac{1}{\pi \cdot RZ2 \cdot fp\_LC}$$

$$CZ2 = \frac{1}{\pi \cdot 4020\Omega \cdot 12kHz} = 6.59nF \approx 6.8nF$$

Calculate **CP1** by placing the first pole at ESR zero frequency

$$CP1 = \frac{1}{2\pi \cdot (Rz2 \cdot fz\_ESR)}$$

$$CP1 = \frac{1}{2\pi \cdot (4020 \cdot 663KHz)} = 59.7\,pF \approx 56\,pF$$

Calculate **RZ3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency

$$RZ3 = \frac{2 \cdot (R1) \cdot (fp\_LC)}{fs - 2\,fp\_LC}$$

$$RZ3 = \frac{2 \cdot (10k\Omega) \cdot (12kHz)}{600KHz - 12kHz} = 408\Omega \cong 400\Omega$$

Calculate **CZ3** from **RZ3** component value above

$$CZ3 = \frac{1}{\pi \cdot RZ3 \cdot fs}$$

$$CZ3 = \frac{1}{\pi \cdot 400\Omega \cdot 600\,KHz} = 1.3nF \approx 1500\,pF$$

Choose 100pF ≤ **CF1** ≤ 220pF to stabilize the SP7661ER internal Error Amplifier. For this example let's select 100pF.

PC LAYOUT DRAWINGS

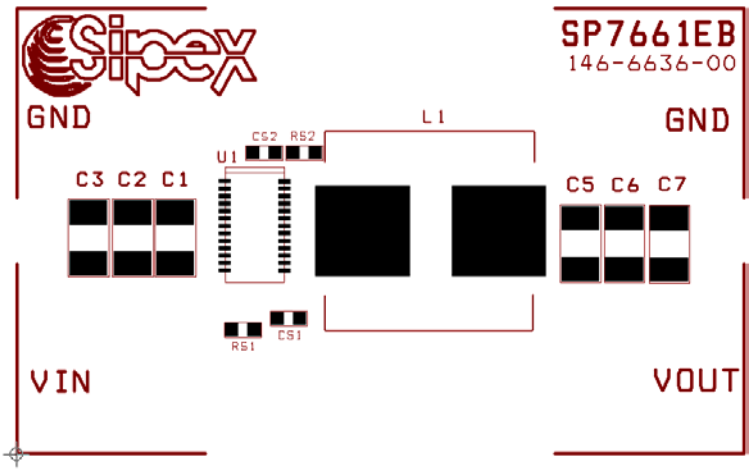


Figure 10. SP7661EB Component Placement

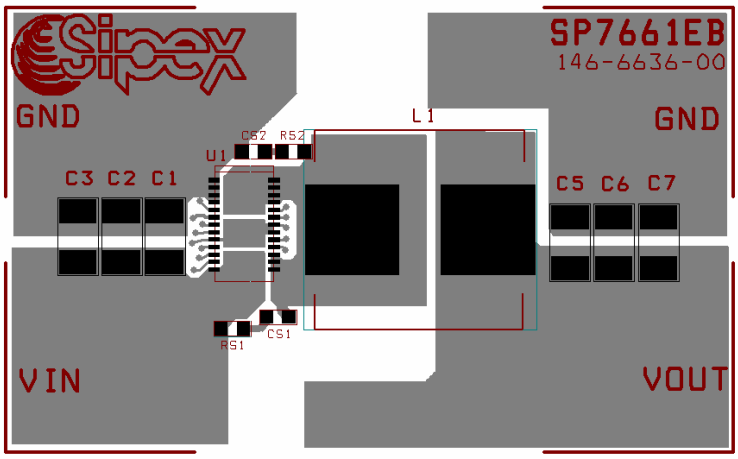


Figure 11. SP7661EB PC Layout Top Side

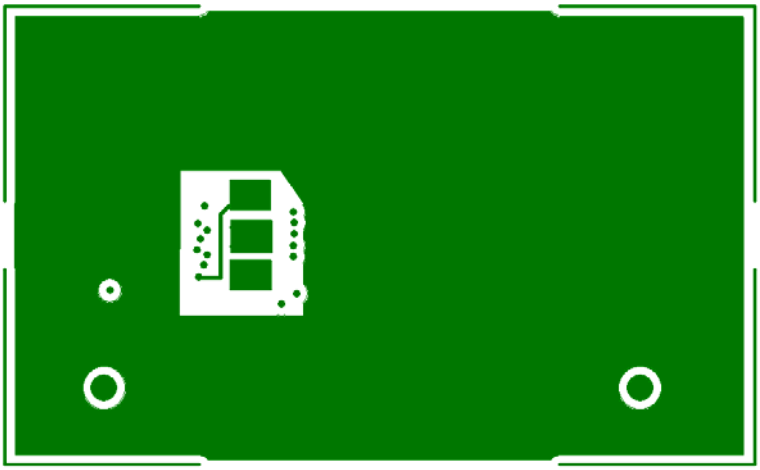


Figure 12. SP7661EB PC Layout 2nd Layer Side

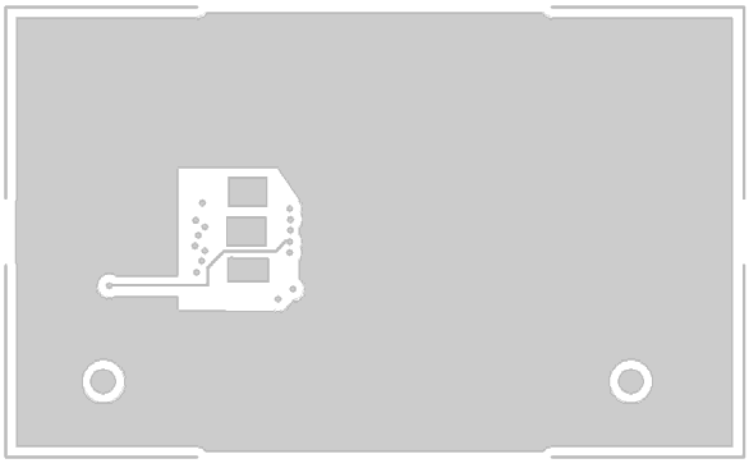


Figure 13. SP7661EB PC Layout 3rd Layer Side

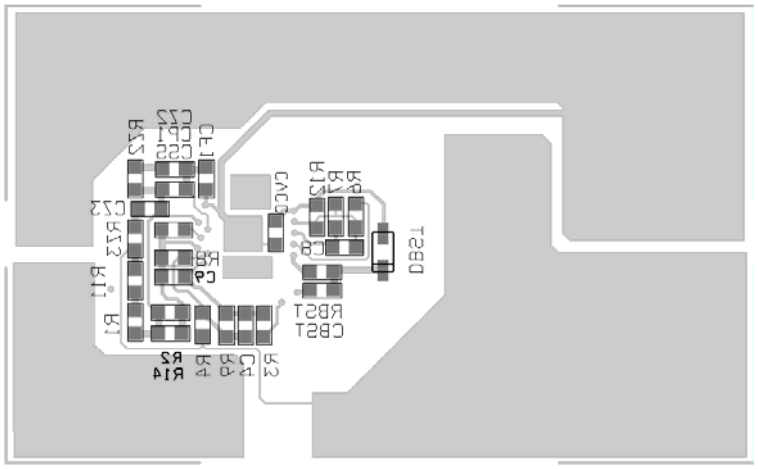


Figure 14. SP7661EB PC Layout Bottom Side

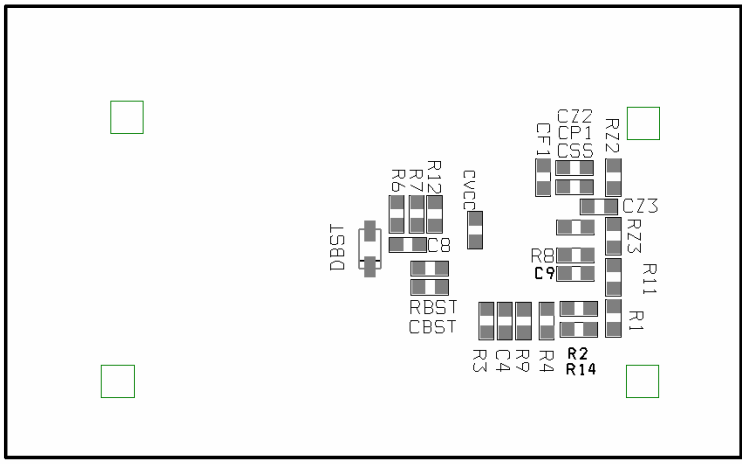


Figure 15. SP7661EB PC Layout Bottom Side Components

Table 1: SP7661EB Suggested Components and Vendor Lists

	7661		12Vin 3V3out				
Line No.	Ref. Des.	Qty.	Manufacturer	Manuf. Part Number	Layout Size	Component	Vendor Phone #
1	PCB	1	Sipex	146-6636-00		SP7661EB	978-667-8700
2	U1	1	Sipex	SP7661EU	DFN-26	Synchronous Buck Regulator	978-667-8700
3	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA-30V Schottky Diode	800-344-4539
4	L1	1	Wurth	744311220	7x7mm	2.2uH Coil, 14mOhm, 9A+	201-785-8800
5	C1, C2	2	Murata	GRM32ER61C226KE20L	1210	22uF Ceramic X5R 16V	770-436-1300
6	C5	1	Murata	GRM31CR60J107ME39L	1206	100uF Ceramic X5R 6.3V	770-436-1300
7	C4,	1	Murata	GRM188R71H473KA93D	0603	47nF Ceramic X7R 50V	770-436-1300
8	CBST	1	Murata	GRM188R71H223KA01D	0603	22nF Ceramic X7R 50V	770-436-1300
9	C9	1	Murata	GRM188R71H682KA01D	0603	6.8nF Ceramic X7R 50V	770-436-1300
10	CVCC	1	TAIYO YUDEN	LMK107BJ475KA-B	0603	4.7uF Ceramic X5R 10V	800-388-2496
11	CF1	1	Murata	GRM1885C1H101JA01D	0603	100pF Ceramic COG 50V	770-436-1300
12	Cs2	1	Murata	GRM1885C1H222JA01D	0603	2.2nF Ceramic COG 50V	770-436-1300
13	CSS	1	Murata	GRM188R71H473KA61D	0603	47nF Ceramic X7R 50V	770-436-1300
14	CP1	1	Murata	GRM1885C1H560JA01D	0603	56pF Ceramic COG 50V	770-436-1300
15	CZ2	1	TDK	C1608CH1H682J	0603	6.8nF Ceramic COG 50V	978-779-3111
16	CZ3	1	Murata	GRM1885C1H152JA01D	0603	1500pF Ceramic COG 50V	770-436-1300
17	R1	1	Panasonic	ERJ-3EKF1002V	0603	10k Ohm Thick Film Res 1%	800-344-4539
18	R2	1	Panasonic	ERJ-3EKF3161V	0603	3.16k Ohm Thick Film Res 1%	800-344-4539
19	R3, R4	2	Panasonic	ERJ-3EKF4991V	0603	5.11k Ohm Thick Film Res 1%	800-344-4539
20	R9	1	Panasonic	ERJ-3EKF6192V	0603	61.9k Ohm Thick Film Res 1%	800-344-4539
21	R11	1	Panasonic	ERJ-3GEYJ00R1V	0603	0 Ohm Thick Film Res 1%	800-344-4539
22	RBST	1	Panasonic	ERJ-3GEYJ00R1V	0603	0 Ohm Thick Film Res 1%	800-344-4539
23	Rs2	1	Panasonic	ERJ-3GEYJ2R0V	0603	1 Ohm Thick Film Res 1%	800-344-4539
24	RZ2	1	Panasonic	ERJ-3EKF4021V	0603	4.02k Ohm Thick Film Res 1%	800-344-4539
25	RZ3	1	Panasonic	ERJ-3EKF4020V	0603	402 Ohm Thick Film Res 1%	800-344-4539
26	VIN, VOUT, GND, GND	4	Vector Electronic	K24C/M	.042 Dia	Test Point Post	800-344-4539

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7661EB	-40°C to +85°C	SP7661 Evaluation Board
SP7661ER	-40°C to +85°C	26-pin DFN(option2)

For further assistance:

Email: Sipexsupport@sipex.com
WWW Support page: http://www.sipex.com/content.aspx?p=support
Live Technical Chat: http://www.geolink-group.com/sipex/
Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx
Type III Loop Compensation Calculator: www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

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