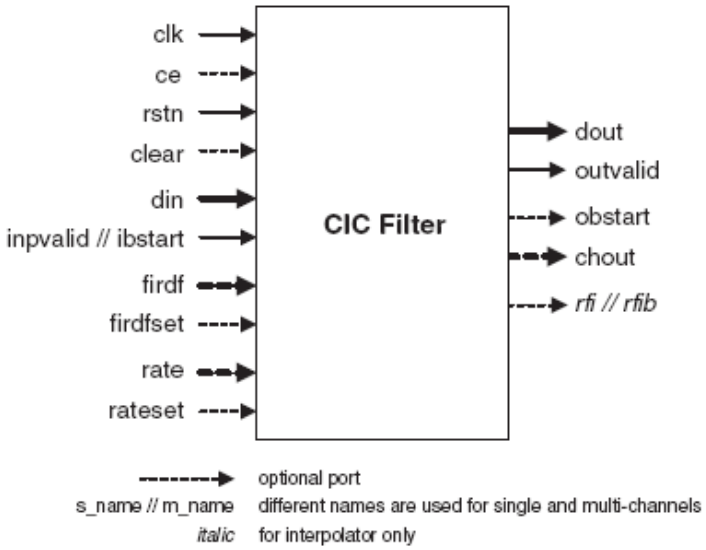
Cascaded Integrator-Comb (CIC) Filter

Overview

Cascaded Integrator-Comb (CIC) filters, also known as Hogenauer filters, are used to achieve arbitrary and large sample rate changes in digital systems. These filters are used as decimation or interpolation filters and can be efficiently implemented without multipliers, utilizing only adders and subtractors.

A CIC filter is typically used in applications where the system sample rate is much larger than the bandwidth occupied by the signal. They are commonly used to build Digital Down Converters (DDCs) and Digital Up Converters (DUCs). Some applications that use the CIC filter include software designed radios, cable modems, satellite receivers, 3G base stations, and radar systems.

Lattice provides a widely parameterizable CIC filter that supports multiple channels with run-time programmable rates and differential delay parameters.



Features

- 1-32-bit Input Data Width
- 1-8 Cascaded Stages
- 1-4 Cycles Differential Delay, Run-time Programmable for Both Decimation and Interpolation
- 2-16,384 Decimation and Interpolation Sampling Rate Factor, Run-time Programmable Rates for Both Decimationand Interpolation
- Multi-channel (up to 4 Channels) Support for Both Decimation and Interpolation
- Fully Synchronous, Single-clock Design

Performance and Resource Utilization

LatticeECP3[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	167	218	301	-	320
Decimator, 16-bit data, 8 stages, 1 channel	873	1588	1253	-	145
Interpolator, 15-bit data, 7 stages, 4 channels	1216	983	1980	-	237

2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2M[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	168	219	301	-	284
Decimator, 16-bit data, 8 stages, 1 channel	878	1589	1253	-	143
Interpolator, 15-bit data, 7 stages, 4 channels	1238	985	1980	-	234

1. Performance and utilization data are generated using an LFE2M-35E-7F672C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	168	219	301	-	272
Decimator, 16-bit data, 8 stages, 1 channel	878	1589	1253	-	144
Interpolator, 15-bit data, 7 stages, 4 channels	1238	985	1980	-	230

1. Performance and utilization data are generated using an LFE2-50E-7F672C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeECP/EC[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	166	216	301	-	212
Decimator, 16-bit data, 8 stages, 1 channel	837	1509	1253	-	109
Interpolator, 15-bit data, 7 stages, 4 channels	1205	898	1980	-	160

1. Performance and utilization data are generated using an LFECP33E-5F672C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP/EC family.

LatticeSC/SCM[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	163	212	301	-	397
Decimator, 16-bit data, 8 stages, 1 channel	839	1510	1259	-	202
Interpolator, 15-bit data, 7 stages, 4 channels	1162	887	1981	-	284

1. Performance and utilization data are generated using an LFSC3GA25E-7F900C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC family.

LatticeXP2[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	168	219	301	-	285
Decimator, 16-bit data, 8 stages, 1 channel	878	1589	1253	-	152
Interpolator, 15-bit data, 7 stages, 4 channels	1238	985	1980	-	234

1. Performance and utilization data are generated using an LFXP2-17E-7F484C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

LatticeXP[1]

Configuration	SLICEs	LUTs	Registers	sysMEM EBRs	f_{MAX}(MHz)
Decimator, 8-bit data, 4 stages, 1 channel	166	216	301	-	196
Decimator, 16-bit data, 8 stages, 1 channel	837	1509	1253	-	103
Interpolator, 15-bit data, 7 stages, 4 channels	1205	898	1980	-	155

1. Performance and utilization data are generated using an LFXP20E-5F484C device, with Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. When using this IP core in a different density, speed, or grade within the LatticeXP family, performance and utilization may vary.

Ordering Information

Family	Part Number
LatticeECP3	CIC-FILT-E3-U2
LatticeECP2M	CIC-FILT-PM-U2
LatticeECP2	CIC-FILT-P2-U2
LatticeECP/EC	CIC-FILT-E2-U2
LatticeSC	CIC-FILT-SC-U2
LatticeXP2	CIC-FILT-X2-U2
LatticeXP	CIC-FILT-XP-U2

IP Version: 3.2
Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.